BANASTHALI VIDYAPITH

Master of Technology (VLSI Design)

Curriculum Structure

First Semester Examination, December, 2020
Second Semester Examination, April/May, 2021
Third Semester Examination, December, 2021
Fourth Semester Examination, April/May, 2022

B**ANASTHALI VIDYAPITH**
P.O. BANASTHALI VIDYAPITH
(Rajasthan)-304022

July, 2020

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No. F. 9-6/81-U.3
Government of India
Ministry of Education and Culture
(Department of Education)

New Delhi, the 25th October, 1983

N O T I F I C A T I O N

In exercise of the powers conferred by Section 3 of the University Grants Commission Act, 1956 (3 of 1956) the Central Government, on the advice of the Commission, hereby declare that Banasthali Vidyapith, P. O. Banasthali Vidyapith, (Rajasthan) shall be deemed to be a University for the purpose of the aforesaid Act.

Sd/-
(M. R. Kolhatkar)
Joint Secretary of the Government of India

N O T I C E

Changes in Bye-laws/Syllabi and Books may from time to time be made by amendment or remaking, and a Candidate shall, except in so far as the Vidyapith determines otherwise, comply with any change that applies to years she has not completed at the time of change.

Programme Educational Objectives

The M.Tech. (VLSI Design) programme aims for the holistic development of students through the unique and innovative fivefold educational ideology of Banasthali Vidyapith. State-of-the-art VLSI technology requires research in physical devices as well as novel design and development of integrated circuits. The M. Tech. (VLSI Design) programme at Department of Electronics aims to impart knowledge of VLSI system design covering algorithms, hardware description languages, system architectures, physical designs, verification techniques, simulation & synthesis, low power design techniques and etc. The programme offers foundational subjects like semiconductor devices, digital, analog and RFIC design, embedded system, electronic system packaging etc. Many courses have prominent lab component, offering hands-on training and exercises on numerous practical spects of crucial importance. The students also get an opportunity to participate in projects related to design and optimization of VLSI circuits and systems.

The main objectives of M. Tech. (VLSI Design) programme are:

- To provide in-depth knowledge of device fundamentals and modern circuits design to gain an ability to analyze, design, and implement VLSI Systems circuits and systems.
- To enrich students to excel in research leading to cutting edge technology in VLSI design to create competent, innovative and productive professionals.
- To train them to understand the various recent issues and find the solutions with good scientific and engineering knowledge, so as to comprehend, analyze, design, and create novel products and develop the capability to prepare the scientist report in lucid and articulate form.
- To provide students with an academic environment to develop scientific awareness, leadership, ethical conduct, positive attitude, societal responsibilities and the lifelong learning needed for a successful professional career.
- To develop entrepreneurial skills in starting industries using VLSI technology.
- Practice the ethics of their profession and inculcate a lifelong learning culture.
- Communicate effectively and manage resources skilfully as members and leaders of the profession.

Programme Outcomes

PO1. **Scholarship of Knowledge:** Acquire in-depth knowledge of VLSI technology in wider and global perspective, with an ability to discriminate, evaluate, analyze, synthesize and integrate for enhancement of knowledge. Graduates will be able to apply the knowledge of computing, mathematics, science and electronic engineering for designing VLSI circuits.

PO2. **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using basic principles of mathematics, science and engineering.

PO3. **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations. Graduates will have an ability to design and conduct experiments, perform analysis and interpret the problems of VLSI design.

PO4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern VLSI tools including modeling to complex engineering activities with an understanding of the limitations.

PO6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8. **Engineering Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9. **Leadership Skills:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects in multidisciplinary environments.

PO12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Curriculum Structure
Master of Technology (VLSI Design)

First Year

Semester - I

Course	Code	Course Name	L	T	P	C*
VLSI	507	Digital CMOS IC Design	4	0	0	4
VLSI	531L	Digital CMOS IC Design Lab	0	0	2	1
VLSI	512	HDL Based System Design	4	0	0	4
VLSI	532L	HDL Based System Design Lab	0	0	6	3
VLSI	516	IC Fabrication Technology	4	0	0	4
VLSI	533L	IC Fabrication Technology Lab	0	0	2	1
VLSI	534P	Minor Project (Part - I)	0	0	2	1
VLSI	536	Solid State Device Modeling and Simulation	4	0	0	4
		Discipline Elective	4	0	0	4
		Semester Total:	**20**	**0**	**12**	**26**

Semester - II

Course	Code	Course Name	L	T	P	C*
VLSI	503	Analog and Mixed Signal IC Design	4	0	0	4
VLSI	503L	Analog and Mixed Signal IC Design Lab	0	0	4	2
VLSI	504	ASIC Design	4	0	0	4
VLSI	505	CAD for IC Design	4	0	0	4
VLSI	505L	CAD for IC Design Lab	0	0	4	2
VLSI	535P	Minor Project (Part - II)	0	0	4	2
VLSI	524	RF IC Design	4	0	0	4
		Open Elective	4	0	0	4
		Semester Total:	**20**	**0**	**12**	**26**

Second Year

Semester - III

Course	Code	Course Name	L	T	P	C*
VLSI	602P	Project (Part - I)	0	0	48	24
		Reading Elective - I	0	0	4	2
		Semester Total:	**0**	**0**	**52**	**26**

Semester - IV

Course	Code	Course Name	L	T	P	C*
VLSI	603P	Project (Part - II)	0	0	48	24
		Reading Elective - II	0	0	4	2
		Semester Total:	**0**	**0**	**52**	**26**

List of Discipline Elective

Course	Code	Course Name	L	T	P	C*
CS	429	Pattern Recognition and Image Processing	4	0	0	4
CS	431	Real Time Systems	4	0	0	4
ELE	502	Discrete Time Signal Processing	4	0	0	4
VLSI	501	Advanced Digital Signal Processing	4	0	0	4
VLSI	502	Advanced Digital System Design	4	0	0	4
VLSI	506	Design of Semiconductor Memory	4	0	0	4
VLSI	510	Embedded System Design	4	0	0	4
VLSI	511	Fault Tolerance in VLSI	4	0	0	4
VLSI	513	High Level System Design and Modeling	4	0	0	4
VLSI	514	High Power Semiconductor Devices	4	0	0	4
VLSI	515	High Speed VLSI Design	4	0	0	4
VLSI	517	Integrated Electronic System Design	4	0	0	4
VLSI	518	Introduction to MEMS	4	0	0	4
VLSI	519	Low Power VLSI Design	4	0	0	4
VLSI	520	Nanoelectronics	4	0	0	4
VLSI	537	Photonics Integrated Circuits	4	0	0	4
VLSI	523	Representation and Analysis of Random Signals	4	0	0	4
VLSI	526	Speech Signal Processing	4	0	0	4

List of Reading Elective

Course	Code	Course Name	L	T	P	C*
VLSI	605R	Advanced Electronic Packaging	0	0	4	2
VLSI	606R	Compound Semiconductor Technology	0	0	4	2
VLSI	601R	High Level Synthesis	0	0	4	2
VLSI	604R	VLSI Testing and Design for Testability	0	0	4	2

List of Online Reading Electives

Digital Image Processing
Organic Electronic Devices

*** L - Lecture hrs/week; T - Tutorial hrs/week; P-Project/Practical/Lab/All other non-classroom academic activities, etc. hrs/week; C - Credit Points of the Course**

Student can opt open (Generic) elective from any discipline of the Vidyapith with prior permission of respective heads and time table permitting.

Every Student shall also opt for:
Five Fold Education: Physical Education I, Physical Education II, Five Fold Education: Aesthetic Education I, Aesthetic Education II, Five Fold Education: Practical Education I, Practical Education II one each semester

Project Evaluation Scheme

Duration	Course Code		Course Name	L	T	P	C
2 Semesters (10 months) 1 July - 30 April	VLSI	602P	Project (Part - I)	0	0	48	24
	VLSI	603P	Project (Part - II)	0	0	48	24

Continuous Assessment (40 Marks)

1. Joining report, brief project outlay	- 10 Marks
2. Synopsis	- 10 Marks
3. Mid-term evaluation by Supervisor	- 10 Marks
4. Further evaluation by Supervisor	- 10 Marks
Total	**- 40 Marks**

End Semester Assessment (60 Marks)

1. Project Report	- 20 marks
2. Presentation	- 20 Marks
3. Viva-voce	- 20 Marks
Total	**- 60 Marks**

Five Fold Activities

Aesthetic Education I/II		Physical Education I/II	
BVFF 101	Classical Dance (Bharatnatyam)	BVFF 201	Aerobics
BVFF 102	Classical Dance (Kathak)	BVFF 202	Archery
BVFF 103	Classical Dance (Manipuri)	BVFF 203	Athletics
BVFF 104	Creative Art	BVFF 204	Badminton
BVFF 105	Folk Dance	BVFF 205	Basketball
BVFF 106	Music-Instrumental (Guitar)	BVFF 206	Cricket
BVFF 107	Music-Instrumental (Orchestra)	BVFF 207	Equestrian
BVFF 108	Music-Instrumental (Sarod)	BVFF 208	Flying - Flight Radio Telephone Operator's Licence (Restricted)
BVFF 109	Music-Instrumental (Sitar)	BVFF 209	Flying - Student Pilot's Licence
BVFF 110	Music-Instrumental (Tabla)	BVFF 229	Aeromodelling
BVFF 111	Music-Instrumental (Violin)	BVFF 210	Football
BVFF 112	Music-Vocal	BVFF 211	Gymnastics
BVFF 113	Theatre	BVFF 212	Handball
Practical Education I/II		BVFF 213	Hockey
BVFF 301	Banasthali Sewa Dal	BVFF 214	Judo
BVFF 302	Extension Programs for Women Empowerment	BVFF 215	Kabaddi
BVFF 303	FM Radio	BVFF 216	Karate - Do
BVFF 304	Informal Education	BVFF 217	Kho-Kho
BVFF 305	National Service Scheme	BVFF 218	Net Ball
BVFF 306	National Cadet Corps	BVFF 219	Rope Mallakhamb
		BVFF 220	Shooting
		BVFF 221	Soft Ball
		BVFF 222	Swimming
		BVFF 223	Table Tennis
		BVFF 224	Tennis
		BVFF 225	Throwball
		BVFF 226	Volleyball
		BVFF 227	Weight Training
		BVFF 228	Yoga

Every Student shall also opt for:
Five Fold Education: Physical Education I, Physical Education II,
Five Fold Education: Aesthetic Education I, Aesthetic Education II,
Five Fold Education: Practical Education I, Practical Education II
one each semester

Evaluation Scheme and Grading System

Continuous Assessment (CA) (Max. Marks)					End-Semester Assessment (ESA) (Max. Marks)	Grand Total (Max. Marks)
Assignment		Periodical Test		Total (CA)		
I	II	I	II			
10	10	10	10	40	60	100

In all theory, laboratory and other non classroom activities (project, dissertation, seminar, etc.), the Continuous and End-semester assessment will be of 40 and 60 marks respectively. However, for Reading Elective, only End semester exam of 100 marks will be held. Wherever desired, the detailed breakup of continuous assessment marks (40), for project, practical, dissertation, seminar, etc shall be announced by respective departments in respective student handouts.

Based on the cumulative performance in the continuous and end-semester assessments, the grade obtained by the student in each course shall be awarded. The classification of grades is as under:

Letter Grade	Grade Point	Narration
O	10	Outstanding
A+	9	Excellent
A	8	Very Good
B+	7	Good
B	6	Above Average
C+	5	Average
C	4	Below Average
D	3	Marginal
E	2	Exposed
NC	0	Not Cleared

Based on the obtained grades, the Semester Grade Point Average shall be computed as under:

$$SGPA = \frac{CC_1 * GP_1 + CC_2 * GP_2 + CC_3 * GP_3 + ---- + CC_n * GP_n}{CC_1 + CC_2 + CC_3 + ---- + CC_n} = \frac{\sum_{i=1}^{n} CC_i * GP_i}{\sum_{i=1}^{n} CC_i}$$

Where n is the number of courses (with letter grading) registered in the semester, CC_i are the course credits attached to the i^{th} course with letter grading and GP_i is the letter grade point obtained in the i^{th} course. The courses which are given Non-Letter Grades are not considered in the calculation of SGPA.

The Cumulative Grade Point Average (CGPA) at the end of each semester shall be computed as under:

$$CGPA = \frac{CC_1 * GP_1 + CC_2 * GP_2 + CC_3 * GP_3 + ----+ CC_n * GP_n}{CC_1 + CC_2 + CC_3 + ----+ CC_n} = \frac{\sum_{i=1}^{n} CC_i * GP_i}{\sum_{i=1}^{n} CC_i}$$

Where n is the number of all the courses (with letter grading) that a student has taken up to the previous semester.

Student shall be required to maintain a minimum of 4.00 CGPA at the end of each semester. If a student's CGPA remains below 4.00 in two consecutive semesters, then the student will be placed under probation and the case will be referred to Academic Performance Review Committee (APRC) which will decide the course load of the student for successive semester till the student comes out of the probationary clause.

To clear a course of a degree program, a student should obtain letter grade C and above. However, D/E grade in two/one of the courses throughout the UG/PG degree program respectively shall be deemed to have cleared the respective course(s). The excess of two/one D/E course(s) in UG/PG degree program shall become the backlog course(s) and the student will be required to repeat and clear them in successive semester(s) by obtaining grade C or above.

After successfully clearing all the courses of the degree program, the student shall be awarded division as per following table.

Division	CGPA
Distinction	7.50 and above
First Division	6.00 to 7.49
Second Division	5.00 to 5.99
Pass	4.00 to 4.99

CGPA to % Conversion Formula: % of Marks Obtained = CGPA * 10

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First Semester

VLSI 507 Digital CMOS IC Design

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Gain in-depth understanding of designing and analysis of CMOS inverters
- Explain the fabrication process and layout design of CMOS digital IC
- To describe the operation of semiconductor memories and low power circuits.

Section-A

CMOS Logic, MOS Inverter, CMOS Inverters, Transmission Gate, MOS Inverter's Switching Characteristics & Interconnect Effects: Delay Time, Interconnect Parasitic, Capacitances (Gate & routing capacitance), Resistance, RC Delay, Wire Delays, Inductances, Gate Delays, Stage Ratio, Power Dissipation, CMOS Logic Gate Design, Transmission Gate, BiCMOS circuits.

Section-B

Combinational Circuits Design: NAND Gate, NOR Gate, Transient Analysis of NAND& NOR gates, Sequential MOS Logic Circuits: Behaviour of Bitable element, pass transistor logic CMOS Latches & Clocked Flip-flop, Clock Skew, Clocking Strategies.

CMOS technology.n-well, pwell process., CMOS process enhancement. Interconnect and circuit elements. Layout design rules. Latch up.

Section-C

CMOS Dynamic Logic Circuit: Transfer; Charge storage and Leakage, Voltage Bootstrapping, High performance dynamic CMOS circuits: Domino CMOS logic, NORA CMOS logic, zipper CMOS circuits, TSPC dynamic CMOS.

Semiconductor Memories: ROM, DRAM, SRAM, PLA, Cell, Leakage Circuit and Input/Output Circuit

Low power circuits: overview of power consumption, low power design through Voltage estimation and optimization of switching activity, reduction of switched capacitor, adiabatic logic circuits.

Recommended Books:

1. Weste, Neil. H. E.,& Eshraghian, K. (1993). *Principles of CMOS VLSI Design.* Boston: New York: Addison Wesley Publication.
2. Weste, Neil. H. E., & Eshraghian, K. (1998). *Principles of CMOS VLSI Design.* Boston: New York: Addison Wesley Publication.
3. Backer, Jacob., Harry, W. Li., & Boyce, David. E. (1999). *CMOS Circuit Design, Layout and Simulation.* New Delhi: PHI Publication.
4. Kang, Sung-Mo., & Leblebici, Yusuf. (2002). *CMOS Digital Integrated Circuits- Analysis and design*. New Delhi: Tata McGraw-Hill Publication.
5. Pucknell, Douglas. A.,& Eshragian, K.(2000). *Basic VLSI Design*. New Delhi: PHI Publication.

Suggested E-resources:

1. **Computation Structures - Part 1: Digital Circuits** by Chris Termanhttps://www.edx.org/course/computation-structures-part-1-digital-mitx-6-004-1x-0
2. **CMOS Digital VLSI Design** by Prof. S. Dasgupta https://onlinecourses.nptel.ac.in/noc19_ee25/preview

VLSI 531L Digital CMOS IC Design Lab

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**0**	**0**	**2**	**1**

Learning Outcomes: After completion of this laboratory course, students will be able to:

- Understand of Cadence circuit design tool
- Understand procedure to analyse DC and Transient behaviour of circuits
- Understand procedure to analyse effects of device dimension variation on circuit performance

List of Experiments:

1. Introduction to Cadence design tool.
2. Comparative study of VI Characteristics of NMOS and PMOS.
3. DC and Transient analysis of CMOS Inverter.
4. Effect of Channel length variation on IO Characteristics of CMOS Inverter.
5. Transient analysis of NAND, NOR Gate.
6. Transient analysis of AND, OR Gate.
7. Transient Analysis of Latch and Flip flop.
8. DC and Transient analysis of CMOS Inverter using symbol.
9. Transient analysis of NAND, NOR, AND, OR gate using symbol.
10. DC and Transient analysis of resistive load Inverter.
11. DC and Transient analysis of buffer circuit.

VLSI 512 HDL Based System Design

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Analysis and Design of Synchronous and Asynchronous sequential machines.
- Draw a FSM chart for digital designs and describe it using HDL.
- Detect and diagnosis different errors in digital circuit descriptions.
- Design the digital systems through VHDL and Verilog HDL.

Section-A

Introduction to hardware design: Digital system design process, hardware description languages, hardware simulation, hardware synthesis, level of abstraction

HDL Background: HDL History, Existing Languages, HDL Requirements, the HDL Language.

Design Methodology Based On HDL: Elements of HDL, Top down Design, Top down Design with HDL, Conventions and Syntax.

Basic concepts of hardware description languages. Hierarchy, Concurrency, Logic and Delay modeling. Structural, Data-flow and Behavioural styles of hardware description. Architecture of event driven simulators.

Section-B

Structural Specification of Hardware: Parts Library, Wiring of Primitives and Iterative Networks, Modeling a Test Bench.

Design Organization and Parameterization: Definition and Usage of Subprograms, Packaging Parts and Utilities, Design Parameterization, Design Configuration, Design Libraries.

Utilities for High-Level Descriptions:

Type Declarations and Usage, VHDL Operators, Subprogram Parameter Types and Overloading, Other Types and Type Related Issues, Predefined Attributes, User Defined Attributes.

Dataflow Descriptions in VHDL: Multiplexing and Data Selection, State Machine Description, Three State Bussing.

Behavioral Description of Hardware: Process Statement, Assertion Statement, Sequential Wait Statements, MSI based design

Section-C

Syntax and Semantics of Verilog.Variable types, arrays and tables. Operators, expressions and signal assignments. Modules, nets and registers, Concurrent and sequential constructs.Tasks and functions, Examples of design using Verilog. Synthesis of logic from hardware description

Introduction: FPGA Design flow, Programmable Technology: Antifuse, Metal-Metal antitfuse, static RAM, EPROM &EEPROM Technology, Specification

Recommended Books:

1. Navabi, Z. (1997) *VHDL: Analysis and Modelling of Digital Systems*. New Delhi: McGraw Hill Publication.
2. Bhaskar, J. (2015). *A VHDL Primer*.New Delhi: Pearson Publication.
3. Lipsett, R., Schaefer, C.,& Ussery, C. (1993) *VHDL Hardware Description and Design*. Menlo Park,California: Kluwer Academic Publishers.
4. Pick, J. (1996) *VHDL: Techniques, Experiments and Caveats*. New Delhi: McGraw Hill Publication.

5. Ott, Douglas E., &Wilderotter, J. *(1994). A Designer's Guide to VHDL Synthesis*. Berlin: Springer.
6. Palnitkar, S. (2003). *Verilog HDL: A Guide to Digital Design and Synthesis*. New Delhi: PHI Publication.
7. Smith, M.J.S. (1997). *Application- Specific Integrated Circuits*.Boston, New York: Addison Wesley Publication.

Suggested E-resource:

1. **Hardware Modeling using Verilog** by Prof.IndranilSengupta, Department of Computer Science and Engineering, Indian Institute of Technology, Kharagpur https://nptel.ac.in/courses/106105165/1

VLSI 532L HDL Based System Design Lab

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**0**	**0**	**6**	**3**

Learning Outcomes: After completion of this laboratory course, students will be able to:

- Describe the IEEE Standard 1076 Hardware Description Language (VHDL).
- Model complex digital systems at several levels of abstractions; behavioural and structural, synthesis and rapid system prototyping.
- Develop and simulate register-level models of hierarchical digital systems.
- Develop a formal test bench from informal system requirements.

List of Experiments:

1. Design all gates using VHDL, and verify functionality through simulation outcomes
2. Write VHDL program for Half adder circuit, and verify functionality through simulation outcomes
3. Write VHDL program for Full adder circuit, and verify functionality through simulation outcomes
4. Write VHDL program for Multiplexer circuit, and verify functionality through simulation outcomes
5. Write VHDL program for Demultiplexer circuit, and verify functionality through simulation outcomes

6. Write VHDL program for encoder circuit, and verify functionality through simulation outcomes
7. Write VHDL program for decoder circuit, and verify functionality through simulation outcomes
8. Write VHDL program for D Flip Flop, and verify functionality through simulation outcomes
9. Write VHDL program for T Flip Flop, and verify functionality through simulation outcomes
10. Write VHDL program for SR Flip Flop, and verify functionality through simulation outcomes
11. Write VHDL program for JK Flip Flop, and verify functionality through simulation outcomes
12. Write VHDL program for modulo 8 up Asynchronous counter circuit, and verify functionality through simulation outcomes
13. Write VHDL program for modulo 8 down Asynchronous counter circuit, and verify functionality through simulation outcomes
14. Write VHDL program for modulo 8 up synchronous counter circuit, and verify functionality through simulation outcomes
15. Write VHDL program for modulo 8 down synchronous counter circuit, and verify functionality through simulation outcomes
16. Write VHDL program for shift and add multiplier circuit, and verify functionality through simulation outcomes
17. Write VHDL program for 4 bit ALU, and verify functionality through simulation outcomes
18. Write VHDL program for parallel adder circuit, and verify functionality through simulation outcomes
19. Write VHDL program for sequence detector circuit, and verify functionality through simulation outcomes
20. Write VHDL program for serial adder circuit, and verify functionality through simulation outcomes

VLSI 516 IC Fabrication Technology

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Understand thin film deposition and vacuum evaporation process.
- Differentiate dry and wet oxidation process and printing methods.
- Perform measurement techniques for extracting electrical properties of devices.
- Understand diffusion and ion implantation process.

Section-A

Crystal Growth & Wafer Preparation, Processing Considerations: Chemical wafer Cleaning, Gettering and Thermal Stress Factors.

Epitaxy: Vapour Phase Epitaxy - basic transport processes and Reaction Kinetics, doping and auto-doping, equipments and safety considerations, buried layers, epitaxial defects, Molecular Beam Epitaxy - equipment used, film characteristics, SOI structures.

Section-B

Oxidation: Growth Mechanism and Kinetics, Silicon Oxidation Model, Interface Considerations, Orientation dependence of Oxidation Rates, Thin and thick Oxides. Oxidation techniques and systems dry & wet Oxidation, Plasma Oxidation, masking properties of SiO2

Lithography: Optical Lithography - Optical resists, contact and proximity printing, projection printing, electron lithography - resists, mask generation. Electron Optics - Roaster scan and Vector scan, variable beam shape, X-ray lithography - resists and Printing, X-ray sources and masks, ion-lithography.

Section-C

Etching: Reactive plasma etching, AC and DC plasma excitation, plasma properties, chemistry and surface interactions, feature size control and anisotropic etching, ion enhanced and induced etching, properties of etch processes. Reactive - Ion - Beam - Etching. Specific etch processes: PolySi/Polycide. Trench etching, SiO_2& $Si_3 N_4$, Diffusion, ion implantation, annealing and sintering, Metalization and pattering. Fabrication steps of NMOS, PMOS, CMOS (n & p well), BJT.

Recommended Books:

1. Sze, Simon. (2017). *VLSI Technology*. New Delhi: McGraw Hill Publication
2. Gandhi, S. K. (1994). *The Theory and Practice of Microelectronics*. New Delhi: John Wiley Publication.
3. Nagchoudhuri, D. (2002). *Microelectronics technology*. New Delhi: Pearson Publication.
4. Chang, C. Y.,& Sze, Simon. (1996). *ULSI Technology*. Singapore,Tata McGraw Hill Publication.

Suggested E-resources:

1. **Introduction to IC fabrication**by Prof. Hardik J Pandya S, Department of Electronic Systems Engineering, IISC, Bangalore. https://nptel.ac.in/courses/108108111/3.
2. **MOSFET Fabrication for IC** by Dr. Nandita Dasgupta Department of Electrical Engineering, Indian Institute of Technology, Madras. https://nptel.ac.in/courses/117106093/3.

VLSI 533L IC Fabrication Technology Lab

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**0**	**0**	**2**	**1**

Learning Outcomes: After completion of this laboratory course, students will be able to:

- Understand fabrication process flow
- Understand Silvaco TCAD tool.
- understand the procedure to modeling devises and analysing their characteristics

List of Experiments:

All experiments will be performed on Silvaco TCAD Tool.

1. Model the fabrication process flow of NMOS with I/V characteristics curve
2. Model the fabrication process flow of PMOS with I/V characteristics curve
3. Model the fabrication process flow of NPN/PNP mos based transistor with input/output characteristics curve.
4. Model the fabrication process flow of PN junction diode.

VLSI 534P Minor Project (Part-I)

Max. Marks : 100	L	T	P	C
(CA: 40 + ESA: 60)	0	0	2	1

Learning Outcomes: After completion of this laboratory course, students will be able to:

- Formulate the project objectives and deliverables.
- Estimate the physical resources required, and make plans to obtain the necessary resources.
- Develop plans with relevant people to achieve the project's goals.

VLSI 536 Solid State Device Modeling and Simulation

Max. Marks : 100	L	T	P	C
(CA: 40 + ESA: 60)	4	0	0	4

Learning Outcomes: After successful completion of this course, students will be able to:

- Explain the carrier densities, charge transport, band diagrams and their relations to the device characteristics.
- Describe the SPICE device models and apply the basic governing model equations to analyse BJT and MOSFET.
- Explain and analyse the operation of optical, microwave and quantum effect devices.

Section-A

Basic Semiconductor Physics: Quantum Mechanical Concepts, Semiconductor materials, Basic Crystal Structure, Valance bonds, Energy bands, Intrinsic Carrier Concentration, Donors and acceptors

Carrier Transport Phenomena: Carrier Drift, Carrier Diffusion, Generation and recombination process, Mobility and Resistively, Continuity equation, Thermionic Emission Process, Tunneling process,

Fermi level, Schottky Barriers and Ohmic Contacts

Section-B

MOSFET and Compound Semiconductor FET:

MOS Capacitor, The MOS diode, MOSFET fundamentals, MOS Transistor current, Threshold Voltage, MOSFET Scaling, Short Channel and narrow width effect, Punch through.

Modeling of MOS: The level 1 Model equation, The level 2 Model equations, the level 3 model equations, Small signal N-Channel MOSFET model, Static n-channel model, MOSFET parameters, Examples of MOSFET Amplifier

Metal -Semi-conductor Constants, MESFET, MODFET

Bipolar Junction Transistor: The transistor action, static Characteristic of Bipolar Transistor, frequency Response and switching of bipolar transistor.

The SPICE BJT Model: Introduction, Small Signal BJT Model, A general large signal Model for the BJT: Ebers-moll (EM) Model and Gummel pool Model, BJT statement, BJT parameters, Examples

Section-C

Optoelectronic devices: photodiode, light emitting diode, Laser-semiconductor laser, hetro-junction laser, material for semi- conductor Laser

Microwave diodes, Quantum effect, hot electron devices: Basic microwave technology, tunnel diode, Impattdiode,Gunn diode transferred electron devices, quantum effect devices, Hot electron devices.

Recommended Books:

1. Sze, S. M. (1985). *Semiconductor Devices Physics and Technology*. New York: Wiley Publication.
2. Streetman, Ben. G.,&Banerjee, Sanjay.Kumar.(2019). *Solid State Electronics Devices*. New Delhi: Pearson Publication.
3. Kang, Sung-Mo., & Leblebici, Yusuf. (2002). *CMOS Digital Integrated Circuits- Analysis and Design*. New Delhi: Tata McGraw-Hill Publication.
4. Smith, Sedra. (2013). *Microelectronics Circuits*. New Delhi: Oxford University Press.

Suggested E-resources:

1. **Solid State Devices** by Dr. S. Karmalkar, Department of Electronics & Communication Engineering, Indian Institute of Technology, Madras. https://nptel.ac.in/courses/117106091/
2. **Semiconductor Devices** by Prof. Dr. G.S. Visweswaran, Department of Electronics & Communication Engineering, Indian Institute of Technology, Delhi. https://nptel.ac.in/courses/117102061/

Second Semester

VLSI 503 Analog and Mixed Signal IC Design

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Design basic cells like current sources, current mirrors and reference circuit.
- Explain stability issues and design compensated IC operational amplifiers.
- Design and analyse comparators and sample-and-hold circuits.
- Illustrate the operation of commonly used data conversion circuits.

Section A

Review of Small Signal MOS Transistor Models, Analog MOS Process, Voltage and Current Sources/sink, Voltage and Current References, Current Mirrors (simple, widler, wilson and cascode), Differential Amplifier,small signal and large signal analysis, non-linear properties, Introduction to analogBiCMOS circuits.

Section B

Operational Amplifier: Theory and Design; Definition of Performance Characteristics; Design of compensated and non-compensated 2-stage CMOS Operational Amplifier, Frequency response, comparators, Analog Buffers, Source Follower.

Section C

Analog Filters (Continuous- time and Switched-Capacitor); Digital Filters, Digital-to-Analog (D/A) and Analog-to-Digital (A/D) Converters. Sample-and-Hold Circuits, Sigma-Delta Converters

Recommended Books:

1. Allen, Phillip.E.,& Holberg, Douglas. R. (2002). *CMOS Analog Circuit Design.* New York: Oxford University Press.
2. Johns, D. A., & Martin, Key (1997). *Analog Integrated Circuit Design*. New York: John Wiley and Sons.
3. Baker, R.J. (2008). *CMOS Mixed Signal Circuit Design*. New York: Wiley/IEEE Press
4. Gregorian, R.,& Temes, G. C.(1986). *Analog MOS Integrated Circuits for Signal Processing*. New York: John Wiley Publication.
5. Gray, Paul. B., & Meyer, Robert.G. (2001). *Analysis and Design of Analog Integrated Circuits*. New York: John Wiley Publication.
6. Geiger, R. L.,Allen, P. E.,&Strader, N. R.(1990). *VLSI Design Techniques for Analog & Digital Circuits*. New Delhi: MGraw Hill Publication.

Suggested E-resource:

1. **Analog Integrated Circuit Design** by Prof. Nagendra Krishnapura, Department of Electrical Engineering, Indian Institute of Technology, Madras. https://nptel.ac.in/courses/ 117106030/

VLSI 503L Analog and Mixed Signal IC Design Lab

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**0**	**0**	**4**	**2**

Learning Outcomes: After completion of this laboratory course, students will be able to:

- Analyse and interpret the waveform, comparison of simulation results with the theoretical analysis.
- Ability to use the simulation software for performing the experiments.
- Ability to design and test various amplifier circuits, which meets the desired specifications.

List of Experiments:

1. Design NMOS simple current mirror for channel length of 1 μm and 180 nm and study DC analysis. Compare the results at two different channel lengths.
2. Analyse AC characteristics of the simple current mirror and determine small signal output resistance. Comparison of small signal resistance at different channel lengths. Discuss the results.
3. Draw the schematic of NMOS CASCODE current mirror for channel length of 1 μm and analyse DC response. Do the same for 180 nm channel length. Compare and discuss the results.
4. Analyse AC characteristics of the CASCODE current mirror and determine small signal output resistance. Comparison the small signal resistance with simple current mirror. Discuss the results.
5. Design CMOS differential amplifier for a given channel length and draw the schematic cell view of differential amplifier.
6. Create the symbol for the differential amplifier and build the differential amplifier test design.
7. Set up and run simulations (AC, DC and Transient) on the Differential Amplifier Test design.
8. Calculate the gain, bandwidth and CMRR of Differential pair. Discuss the results.
9. Design of current source loaded common source amplifier. Create a new cell view and build Common Source Amplifier. Create a symbol for the Common Source Amplifier
10. Build CS_amplifier_test circuit using your CS_amplifier, set up and run simulations (AC, DC and Transient) on the CS_amplifier_test design.
11. Determine the gain, bandwidth and voltage swing of CS amplifier. Comment on the results.
12. Create a new cell view and build Common Drain (CD) Amplifier. Build CD amplifier test circuit using your CD amplifier. Set up and run simulations (AC, DC and Transient) on the CD amplifier test design.
13. Determine the gain, bandwidth and voltage swing, output resistance of CS amplifier. Comment on the results.

14. Build schematic capture of two stage operational amplifier (OP-AMP) using the previously created symbols of CS amplifier and CD amplifier. Thereafter create a symbol for the OP-AMP.
15. To build op-amp_test circuit using your op-amp. Set up and run simulations (AC, DC and Transient) of op-amp_test circuit.
16. Determine voltage gain, slew rate, UGB and Phase Margin of two stage Op-Amp and compare with the design specifications. Comments on the results

VLSI 504 ASIC Design

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Analyze the concept of Full Custom ASIC and Semi-Custom ASIC, Cell Libraries, Data Logic Cells, Low-level Design Entry and Low Level Design Languages
- Explain ASIC I/O Cell: DC Output, AC Output, DC Input, AC Input, Clock Input, Power Input and PLA Tools.
- Describe Programmable ASIC Logic Cell, FPGA Logic Cells, and Programmable Interconnects to Solve the RC delay of routing resources for each ASIC.

Section-A

Introduction: Full Custom with ASIC, Semi-custom ASICS, Standard Cell based ASIC, Gate array based ASIC, Channeled gate array, Channel less gate array, structured get array, Programmable logic device, FPGA design flow, ASIC cell libraries

Data logic cells: Data Path Elements, Adders, Multiplier, Arithmetic Operator, I/O cell, Cell Compilers

ASIC library Design: Logical effort: practicing delay, logical area and logical efficiency logical paths, multi stage cells, optimum delay, optimum no. of stages, library cell design.

Low-level design entry: Schematic Entry:

Hierarchical Design. The cell library, Names, Schematic, Icons & Symbols, Nets, schematic entry for ASIC'S, connections, vectored instances and buses, Edit in place attributes, Netlist, screener, Back annotation

Section-B

Programmable ASIC logic cell, ASIC I/O cell (DC output, AC output, DC input AC Input, Clock input. Power input, Xilinx I/O black, other I/O block).

A brief introduction to low-level design language, EDIF, PLA Tools, an introduction to CFI designs representation.

Section-C

FPGA Basic Logic Cells: Actel Act: Shannon's expansion theorem, ACTI, ACT2, ACT3 logic Modules.

Xilinx LCA: XC3000 CLB, XC4000 series, XC 5200 series.

Altera FLEX: FLEX 8000 series logic expenders, timing model, and comparison chart of logic cells.

FPGA interconnect: Actel ACT: Routing recourses, Elmore's constant, RC delay in Antifuse connection, ACT2 ACT 3 interconnect Xilinx LCA, Xilinx EPLD, Altera MAX 5000 and 7000, Altera max 9000, Altera FLEX.

Recommended Books:

1. Smith M. J. S. (2006). *Application Specific Integrated Circuits* USA:Pearson Publication
2. Ismail, Mohammed. &Terri, Fiez. (1994). *Analog VLSI signal and Information processing*. New York: McGraw-Hill Publication.
3. Wolf,Wayne. (2005). *FPGA based System Design*. New Delhi: PHI Publication.
4. Brown, Andrew. (1991). *VLSI Circuits and Systems in Silicon*. New York: McGraw-Hill Publication.
5. Haskard, Malcom. R., & May, Lan C. (1998). *Analog VLSI Design - NMOS and CMOS*. New Delhi: PHI Publication.
6. Geiger, Randall. L., Allen, Phillip E., & Strader, Noel.K. (1990). *VLSI Design Techniques for Analog and Digital Circuits*. New Delhi: PHI Publication.
7. France, Jose.E.,& Tsividis,Yannis. (1994). *Design of Analog-Digital VLSI Circuits for Telecommunication and Signal Processing*. New Delhi: PHI Publication.

8. Brown, S.D., Francis, R.J., Rox, J., &Uranesic, Z.G. (1992). *Field Programmable Gate Arrays*. Menlo Park, California: Kluwer Academic Publishers.

Suggested E-resource:

1. **Digital VLSI Systems Design** by Prof. S. Srinivasan, Department of Electrical Engineering, Indian Institute of Technology, Madras. https://nptel.ac.in/courses/117106092/

VLSI 505 CAD for IC Design

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Understand Basic concept of describing VLSI design problems
- Understand graph theory and its utilization in finding solution for VLSI design problems.
- Understand algorithms to solve various VLSI design problem like floorplaning, scheduling, placement, routing etc.

Section A

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

Graph Optimization Problems and Algorithms:-The shortest and longest path problems, Clique Covering and Clique Partitioning

Boolean Algebra and Applications:-Boolean functions and their representations (Tabular Forms, Expression Forms and Binary decision Diagrams-OBDD, ROBDD)

Abstract Models: - Structures, Logic Networks, State Diagram, Data flow and Sequencing Graph.

Section B

Architectural-Level Synthesis and Optimization:-Introduction, Circuit Specification for Architectural Synthesis, the Fundamental Architectural Synthesis Problems, Area and Performance Estimations, Strategies for Architectural Optimization

Scheduling Algorithms:-A model for the Scheduling Problems, Scheduling without Resource Constraints, Scheduling with Resource Constraints (ILP, LIST, FDS)

Two-Level Synthesis and Optimization: - introduction, Logic optimization Principles

Section C

VLSI PHYSICAL DESIGN:-**Layout Compaction - Design rules** - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning

Floorplanning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

Recommended Books:

1. Gerez, S.H. (2002). *Algorithms for VLSI Design Automation*. New York: John Wiley Publication.
2. Sherwani, N.A. (2002). *Algorithms for VLSI Physical Design Automation*. Boston, New York: Kluwar Academic Publishers.
3. Drechsler, R. (1998). *Evolutionary Algorithms for VLSI CAD*. Boston, New York: Kluwer Academic Publishers.
4. Hill, D., Shugard, D., Fishburn, J.,& Keutzer, K. (1989). *Algorithms and Techniques for VLSI Layout Synthesis*. Boston, New York: Kluwer Academic Publishers.
5. Micheli, Giovanni.De.(2003). *Synthesis and Optimization of Digital Circuits*. New Delhi: TMH Publication.

Suggested E-resource:

1. **CAD for VLSI Design I** by Prof. Prof. V. Kamakoti and Prof Shankar Balachandran, Department of Computer Science and Engineering, Indian Institute of Technology, Madras https://nptel.ac.in/courses/106106088/

VLSI 505L CAD for IC Design Lab

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40 + ESA: 60)	**0**	**0**	**4**	**2**

Learning Outcomes: After completion of this laboratory course, students will be able to:

- Understand the VLSI design automation.
- Understand the process to develop and analyse synthesis outcomes.
- Demonstrate knowledge of computational and optimization algorithms and tools, applicable to solving CAD related problems.

List of Experiments:

1. NETLIST generation and analysis of Half Adder
2. NETLIST generation and analysis of Full Adder
3. NETLIST generation and analysis of Half Subtractor
4. NETLIST generation and analysis of Full Subtractor
5. NETLIST generation and analysis of Multiplexer
6. NETLIST generation and analysis of Demultiplexer
7. NETLIST generation and analysis of D Flip Flop
8. NETLIST generation and analysis of T Flip Flop
9. NETLIST generation and analysis of JK Flip Flop
10. NETLIST generation and analysis of SR Flip Flop
11. NETLIST generation and analysis of Four bit Binary Counter
12. NETLIST generation and analysis of Serial in Serial Out Shift Register
13. NETLIST generation and analysis of Parallel in Serial Out Shift Register
14. NETLIST generation and analysis of Serial in Parallel Out Shift Register
15. NETLIST generation and analysis of Ripple Carry Adder

VLSI 535P Minor Project (Part-II)

Max. Marks : 100	L	T	P	C
(CA: 40 + ESA: 60)	0	0	4	2

Learning Outcomes: After completion of this laboratory course, students will be able to:

- Identify, formulate, and solve VLSI design problems using advanced level manufacturing and design techniques
- Apply advanced level knowledge, techniques, skills and modern tools of VLSI Design.
- Understand the complexities and design methodologies of current and advanced VLSI design technologies.

VLSI 524 RF IC Design

Max. Marks : 100	L	T	P	C
(CA: 40 + ESA: 60)	4	0	0	4

Learning Outcomes: After successful completion of this course, students will be able to:

- Understand basics concepts of radio frequency integrated systems and their performance parameters.
- Identify design trade-off used in various transmitters and receivers architecture with wireless standards.
- Perform VLSI implementation of oscillators, Mixers and Power amplifiers.

Section-A

Introduction to RF and Wireless Technology: Complexity, design and applications. Choice of Technology. Basic concepts in RF Design: Nonlinearly and Time Variance, intersymbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion.

Analog and Digital Modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and Non coherent defection.Mobile RF Communication systems and basics of Multiple Access techniques. Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters.

Section-B

BJT and MOSFETbehavior at RF frequencies Modeling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated Parasitic elements at high frequencies and their monolithic implementation.

Basic blocks in RF systems and their VLSI implementation : Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off.ResonatorlessVCO design. Quadrature and single-sideband generators,

Section-C

Radio Frequency Synthesizes: PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifiers design. Linearisation techniques, Design issues in integrated RF filters.

Some discussion on available CAD tools for RF VLSI designs.

Recommended Books:

1. Razavi, B. (2011). *RF Microelectronics*. New Delhi: PHI Publication.
2. Lee,T.H. (1998). *The Design of CMOS Radio-Frequency Integrated Circuits*. New York: Cambridge University Press.
3. Baker, R.Jacob., Li, H.W., & Boyce, D.E. (1998). *CMOS Circuit Design, Layout and Simulation*. New Delhi: PHI Publication.
4. Tsividis, Y.P. (1996). *Mixed Analog and Digital VLSI Devices and Technology*. New York: McGraw Hill Publication.

Suggested E-resources:

1. **RF System - Basic Architectures** by Prof. Dr. S. Chatterjee, Department of Electrical Engineering Indian Institute of Technology, Delhi. https://nptel.ac.in/courses/117102012/.
2. **RF integrated Circuits** by S. Aniruddhan, Department of Electrical Engineering, IIT Madras.http://www.ee.iitm.ac.in/ ~ani/2011/ee6240/pdf/ee6240_lec32.pdf.

Third Semester

VLSI 602P Project (Part-I)

Max. Marks : 100	L	T	P	C
	0	0	48	24

Learning Outcomes: After successful completion of this course, students will be able to:

- Recognize the need to engage in lifelong learning through continuing education and research.
- Formulate the project objectives and deliverables.
- Estimate the physical resources required, and make plans to obtain the necessary resources.
- Develop plans with relevant people to achieve the project's goals.

Fourth Semester

VLSI 603P Project (Part-II)

Max. Marks : 100	L	T	P	C
	0	0	48	24

Learning Outcomes: After successful completion of this course, students will be able to:

- Demonstrate knowledge of contemporary issues in the area of VLSI design.
- Manage projects related to VLSI design in multidisciplinary environments.
- Understanding the Functioning with multidisciplinary teams, working cooperatively, respectfully, creatively and responsibly as a member of a team.

Discipline Electives

CS 429 Pattern Recognition and Image Processing

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to

- Explain the concept of Image Processing, Mathematical preliminary of Image Processing and various Image Representations.
- Analyse the methods of Image Enhancement and Image Filtering.
- Identify different image analysis and pattern recognition methods and apply them in problem areas also develop an abundance of Image Processing applications that can serve mankind with the available and anticipated technology in the near future.

Section-A

Image processing: introduction, linear systems, the Fourier transform, matrix theory results. Image perception, image sampling, Quantisation: the optimal mean square (Lloyd-max quantiser), visual quantization. Image transforms: two dimensional orthogonal and unitary transforms, properties, one dimensional discrete Fourier transform (DFT), two dimensional DFT, cosine transform, sine transform.

Section-B

Image enhancement: point operation, histogram modeling, spatial operations, transform operation, multispectral image enhancement, false color and pseudocolor, color image enhancement. Image filtering: image observation models, inverse and Wiener filtering, finite impulse response (FIR) wiener filtering, other Fourier domain filters.

Section-C

Image Analysis: Feature extraction, Edge detection, Scene segmentation and labeling. Pattern recognition: Introduction, Recognition process, Statistical decision making (Bayes' theorem), Nonparametric decision making (Nearest neighborhood classification tech), clustering.

Recommended Books:

1. Jain A. K. (2015). *Fundamentals of Digital Iimage Processing*. New Delhi: PHI Publication.

2. Rafel, Gozalez., & Richard, Woods. (2016). *Digital Image Processing*. New Delhi: Pearson Publication.
3. Rosenfield, A., & Kak, A. C.(1982). *Picture Processing*. Orlando: Florida: Academic Press.
4. Pratt, W. K. (2007). *Digital Image Processing*. Hoboken: New Jersey: John Willey and sons, Publication.
5. Friedman, Manahem., & Kandel, Abraham.(1999). *Introduction to Pattern Recognition*. Singapore: World Scientific.
6. Charniak, E.,& Mcdermott, D. (1985). *Introduction to Artificial Intelligence*. Boston: New York: Addison Wesley.

Suggested E-resources:

1. **Pattern Recognition and Application** by Prof. P. K. Biswas, Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology, Kharagpur. https://nptel.ac.in/courses/117105101/

CS 431 Real Time Systems

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- To present the mathematical model of the system.
- Analyse multi task scheduling algorithms.
- To explain Reliability Evaluation techniques and Real time communication algorithms.

Section-A

Introduction to Real-time computing: Characterizing Real-time system & tasks; Performance measures of real time systems, estimation of program run time, Real-time system design: Hardware requirement, system-development cycle, data transfer techniques, synchronous & asynchronous data communication, standard interfaces.

Section-B

Task Assignment and Scheduling: Priority scheduling, scheduling with fixed priority dynamic priority scheduling, Real-time programming languages & Tool: desired language characteristics, data typing, control

structure, run time error handling, overloading & generics, run time support, Real-time databases.

Section-C

Real time communication algorithms, Fault tolerance techniques: Causes of failure, fault types, fault detection, redundancy, integrated failure handling Reliability Evaluation techniques: Parameter values, reliability model for hardware redundancy, software error model, Clock synchronization.

Recommended Books:

1. Krishna, C.M., & Shen, K.G. (2008). *Real Time Systems*. New Delhi: McGraw Hill Publication.
2. Lawrence, P.D., & Mauch, K.(1998). *Real Time Microcomputer Design: An Introduction*. New York: McGraw Hill Publication.
3. Mathai, Joseph.(1996). *Real Time systems: Specification, Verification & Analysis*. London, PHI Publication.
4. Stuart, Bennet.(1994). *Real Time Computer Control*. *,New Jersey:* PHI Publication.

ELE 502 Discrete Time Signal Processing

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Apply discrete-time signal processing techniques analysis to perform various signal operations.
- Apply the principles of Fourier transform analysis to describe the frequency, and characteristics of discrete-time signals and systems.
- Understand the design techniques of various digital and analog filters.

Section A

General concepts of Digital processing: Typical Signal processing operation, example of typical signals, signal processing application basic elements of DSP, overview of DSP systems, Advantages and disadvantages of DSP.Time domain Characteristic of Directed time System: Elementary sequences like unit sample , unit modulation ,addition, multiplication, delay

and advance, Classification, of discrete time system in terms of linearity, time invariance ,causality, stability and passivity; input output relationship and impulse response, response of LTI to any input, Convolution sum and its properties, Cascade and Parallel interconnection of LTI system, stability and response type of LTI system, constant coefficient difference equation for LTI system and its solution using homogenous and particular solution.

Section B

Transform domain analysis of LTI systems: Frequency response, frequency domain characterization of LTI system, transfer (Systems) function, derivation of transfer function (Using difference equation) interrelation, between frequency response and transfer function of higher order filters (cascaded section) Comb filter, zero phase and linear phase FIR transfer functions, all pass transfer function and its properties, minimum phase transfer function, stability test using stability triangle, stability test procedure.

Discrete Fourier Transform : Review of discrete Fourier transfer, DFT as a linear transformation, circular shift and circular convolution of sequences, use of DFT in linear filtering of long data sequences, overlap-save and overlap method, add method, Goertzel and chirp z transform algorithms, radix 2 and radix 4 decimation in time and decimation in frequency FFT algorithm.

Section C

Structures for discrete time system: Basic building block of a discrete time system, pick off node, adder, multiplier, unit delay, structures for FIT systems, direct form, cascaded form frequency sampling and lattice transposed structures, cascade form, parallel form and lattice -ladder structure.

Design of filters: Digital filter specification and selection, FIT filter

Design using window (fixed and adjustable), frequency Sampling approach and Chebyshev approximation method: Design of IIR filter from analog filters using impulse invariance

and Bi-linear transformation technique; Frequency transformation (to low-pass, high-pass, band-pass) in analog and digital domain.

Introduction to Multi-rate Digital Signal Processing: Needs of multi- rate DSP, Sampling rate conversion by a factor I/D Filter and implementation for sampling rate conversion of low-pass signals.

Recommended Books:

1. Proakis, J.G.& Manolakis, D.G. (2014). *Digital Signal Processing: Principles, Algorithms and Applications*.New Jersey: Pearson Publication.
2. Nagarath, I.J.,Sharan, S.N.,Ranjan, R.,& Kumar, S. (2009). *Signals and Systems*, New Delhi: TMH Publication.
3. Oppenheim, A.V., Schafer, R.W., & Buck, J.R. (1998). *Discrete-Time Signal Processing*. New Jersey: PHI Publication.

Suggested E-resources:

1. **Discrete Time Signal Processing** by Prof. Mrityunjoy Chakraborty, Department of Electronics and Electrical Communication Engineering Indian Institute of Technology, Kharagpur. https://nptel.ac.in/courses/117105134/.
2. **Digital Signal Processing** by Prof: S. C. Dutta Roy, Department of Electrical Engineering Indian Institute of Technology, Delhi. https://nptel.ac.in/courses/117102060/.

VLSI 501 Advanced Digital Signal Processing

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Modelling of random filter and identification of different parameters.
- Realization of Kalman filters and concept of spatial smoothing.
- Adaptive implementation of wiener filter and Adaptive noise cancelling.

Section A

Modeling of filter: power Spectrum: sample random filter order: Markov parameter; identification linear prediction and signal modeling; minimal phase signals and filter, minimum delay property; spectral factorization theorem

Section B

Linear estimation: Linear estimation of signals; Stationary Wiener filters; Kalman filter; Construction of Wiener filter, Kalman filter.

Linear prediction: Auto representative model levenson - Analysis and synthesis of lattice filters; Schur algorithm - FIR Wiener filter least square wave shaping and spiking filters. Spectrum estimation: Spectrum estimation by auto regressive modeling; spectral analysis of sinusoids in noise Maximum likely-hood method; spatial smoothing.

Section C

Adaptive filters: Adaptive implementation of wiener filter; Adaptive linear combiner; Adaptive FIR Wiener filter ; Adaptive Channel equalizer; Adaptive echo canceling; Adaptive noise canceling ; Adaptive linear prediction.

Recommended Books:

1. Orfanids, S.J. (1988). *Optimum Signal Processing: An Introduction*. New York: Collier Macmillan Publication.

Suggested E-resource:

1. **State space Models** by Professor Anna Mikusheva Paul Schrimpf. https://ocw.mit.edu/courses/.../14.../MIT14_384F13_lec21.pdf
2. **Adaptive signal Processing** by Prof. Mrityunjoy Chakraborty, Indian Institute of Technology, Kharagpur. https://nptel.ac.in/ courses/117105075/5

VLSI 502 Advanced Digital System Design

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Formulate and solve problems in Digital Systems design.
- Knowledge about the properties of symmetric networks and apply threshold logic on digital circuits.
- Analyze digital system design using PLD.

Section-A

Basic theorems: Shannon's expansion theorem, consensus theorem, octal designation, Reed Murler expansion, Ex-OR Operations, Inhibit & Inclusion & Inclusion operations.

Isomorphic system: Synthesis of multiple output combinational logic by product method.

Minimization method: Prime implicates, Quine-McCluskey decomposition method.

Section-B

Contact Network: Analysis and synthesis: Series parallel network.

Decomposition: Functional decompositions, decomposition by expansion, test for decomposability, decomposing charts.

Symmetric Network: Properties, synthesis, Identification of symmetric.

Threshold logic: Concept capabilities & limitations, properties, synthesis, Linear-Reparability, Identification & realization.

Section-C

Finite state machine: Mealy & Moore model, capabilities and limitation, state equivalence and machine minimization, incompletely specified machine.

Asynchronous sequential circuits: Fundamental mode, synthesis, state assignment, pulse mode circuit, essential hazard & dynamic hazard.

PLA: Introduction, minimization, PLA folded, Maximum folded large PLA's.

Recommended Books:

1. Biswas, Nripendra.N. (2001) *Logic Design theory*. New Delhi: PHI Publication.
2. Kohavi, ZVI. (2010) *Switching and Finite Automata theory*. New York: Cambridge University Press.
3. Fletcher, William. I. (1997) *An Engineering Approach to Digital Design*. New Delhi: PHI Publication.
4. Geiger, Randall. L., Phillip E. Allen., & Strader, Noel. R. (1989) *VLSI Design Techniques for Analog and Digital Circuits*. Boston, Massachusetts: McGraw Hill Publication.

Suggested E-resources:

1. **Programmable logic devices** Prof. D. Roychoudhury Department of Computer Science and Engineering Indian Institute of Technology, Kharagpur. https://nptel.ac.in/courses/117105080/26.
2. **Digital Systems Design** with PLDs and FPGAs Kuruvilla Varghese Department of Electronic Systems Engineering Indian Institute of Science, Bangalore. https://nptel.ac.in/ courses/117108040/.

VLSI 506 Design of Semiconductor Memory

Max. Marks : 100	L	T	P	C
(CA: 40+ ESA: 60)	4	0	0	4

Learning Outcomes: After successful completion of this course, students will be able to:

- Know about architecture of semiconductor memories and methodologies adopted in data storage.
- Analyze the difference in volatile and non-volatile memory, and their building blocks.
- Know memory fault tolerance and testing methodology.

Section A

Random Access Memory Technologies

Static Random Access Memories (Srams): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-BipolarSRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs.

Dynamic Random Access Memories (Drams): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS,DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application Specific DRAMs.

Section B

Nonvolatile Memories : Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-GateEPROM Cell-One-Time Programmable (OTP) Eproms-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture. Memory Fault Modeling, Testing, And Memory Design For

Testability And Fault Tolerance, RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing

Section C

Semiconductor Memory Reliability and Radiation Effects

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability-Reliability Test Structures-Reliability Screening andQualification. RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-NonvolatileMemory Modelling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

Recommended Books:

1. Betty, Prince. (1996). *Semiconductor Memories: A Handbook of Design, Manufacture and Application.* New York: Willey Publication.

Suggested E-resources:

1. **Design of memory circuits** by Prof. D Roychoudhry Department of Computer Science and Engineering Indian Institute of Technology, Kharagpur. https://nptel.ac.in/courses/117105080/31.

VLSI 510 Embedded System Design

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Explain the challenges in the design of embedded system
- Describe the Hardware and Software Tools for Embedded System
- Describe the Features of OS and language for Embedded System

Section A

Introduction to Embedded Systems; Design Challenges: Optimizing Design Metrics; Processor Technology - General Purpose, Single Purpose and Application-Specific Processors; Architectural Issues: RISC, CISC and VLIW Architectures; Custom Single Purpose Processor Design - Combinational, Sequential and RT-Level Components; Design of Controller and Datapath using Sequential Program / FSMD; RT-Level Single-Purpose Processor Design;

Optimizing Custom Single-Purpose Processors; Application Specific Instruction Set Processors (ASIPs) - Microcontrollers, DSPs; Standard

Single -Purpose Processors: Timers, Counters, Watchdog Timers; UART, PWM, LCD Controller, Keypad Controller, Stepper Motor Controller, A2D Converters, Real Time Clocks.

Section B

Types of Memories for Embedded Systems; Component Interfacing: Interrupts, DMA, I/O Bus Structures, Communication Protocols; Introduction to IC Technologies: VLSI, ASIC and PLD IC Technologies; Basic Hardware and Software Tools for Embedded System Design: Linker, Loader, Assembler, Compiler, Simulator, Emulator, In System Programmer, Logic Analyzer etc.

Section C

Digital Camera Example for various Embedded System Implementations; Features of OS for Embedded Systems, Real Time Issues, Windows CE and QNX; Features of Languages for Embedded Systems Specification; Use of UML, Features and difference between VHDL, Verilog and SystemC; Introduction to Generic Co-design Methodology; Testing for Embedded Systems.

Recommended Books:

1. Wolf, M. (2012). *Computers as components: principles of embedded computing system design*. Elsevier.
2. Vahid, F., & Givargis, T.D.(2002) *Embedded System Design:A unified Hardware/ software Introduction.* New Jersey: Wiley Publication.
3. Gannsle, J. (2008) *The Art of Designing Embedded System*. New Delhi: Newnes Publication.
4. Staunstrup, J.,& Wolf,W. (1997) *Hardware /software Codesign: Principles and Practice.* Boston, Massachusetts: Springer Publications.
5. Gajski, D.D., Vahid, F., Narayan, S., & Gong, j. (2007). *Specification design of Embedded System.* New Delhi: Pearson Education India.

Suggested E-resources:

1. **Embedded Systems - Shape The World: Microcontroller Input/Output** by The University of Texas at Austin (UTAustinX), https://www.edx.org/course/embedded-systems-shape-the-world-microcontroller-inputoutput

2. **Embedded Systems** by Georgia Tech as CS, 8803 https://in.udacity.com/course/embedded-systems--ud169
3. **Embedded System Design** with ARM by Dr. Kamalika Datta Indian Institute of Technology, Kharagpur, https://onlinecourses. nptel.ac.in/noc19_cs22/preview

VLSI 511 Fault Tolerance in VLSI

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Diagnose and measure different type of Faults.
- Explain the detection, correction techniques and fault-tolerant networks
- Analyze fault tolerance strategies and enhance capabilities about applications of fault tolerant designs in arithmetic units and systems.
- Explain the basic mechanisms of fault-tolerance methods and fault tolerant computer systems.

Section A

Motivation of fault tolerance in arithmetic systems.Fault and error models in VLSI arithmetic units.Reliability and fault tolerance definitions.Reliability and availability modeling, Estimation of the reliability and availability of fault tolerant systems Fault diagnosis. Fault tolerance measurement. Fault tolerance strategies: detection, correction, localization, reconfiguration. Error recovery, Error detecting and correcting codes

Section B

Detection/correction techniques: modular redundancy, time redundancy (e.g., RESO, RERO, REDWC, RETWV, REXO), datacoding (e.g., AN codes, residue codes, GAN codes, RBR codes, Berger codes, residue number systems), algorithm-based techniques. Reconfiguration techniques.

Applications to arithmetic units and systems (e.g., convolvers, inner product units, FFT units, neural networks). Application levels: unit, processing element, subsystem, system. Cost/benefit analysis. Fault-tolerant transaction processing systems.Fault-tolerant Networks. Redundant disks (RAID).

Section C

Software reliability models, Software fault-tolerance methods: N-version programming, recovery blocks, rollback and recovery

Architecture and design of fault tolerant computer systems using protective redundancy

Recommended Books:

1. Nelson, Victor. P.,&Carroll, Bill. D. (1987). *Tutorial: Fault-Tolerant Computing*, Maryland: IEEE Computer Society Press.
2. Pradhan, D.K. (1996). *Fault Tolerant Computer System Design*. New Jersey: PHI Publication.
3. Johnson, B.W. (1989) *Design and Analysis of Fault-Tolerant Digital Systems*. Boston, Massachusetts: Addison-Wesley.

Suggested E-resources:

1. **VLSI Design Verification and Test** by Prof. Jatindra Kumar Deka and Dr. Santosh Biswas, Department of CSE, IIT Guwahati. https://nptel.ac.in/courses/106103016/

VLSI 513 High Level System Design and Modeling

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Understand describing a system
- Understand about information system and models
- Understand system analysis and system design

Section A

Introduction to Design Representation of Digital Systems, levels of abstraction, design methodologies, System level methodologies, System specification and design.

Model Taxonomy: State-Oriented models - finite-state machine, Petri net, Hierarchical concurrent finite state machine; Activity-oriented models - Dataflow graph, flow charts; Heterogeneous model - control/data flow graph, Object oriented model, Program-state machine;

Architectural Taxonomy: Application specific architectures - Controller Architecture, Data path architecture, Finite-state machine with data path;

Processors - Complex instruction set Computer, Reduced instruction set Computer; Vector machine - Very long instruction word Computer; Parallel processors.

Section B

A Specification example of Telephone answering machine : Specification capture with spec-charts, Sample test bench, Advantage of executable specifications; Strengths of the PSM model - Hierarchy, State transitions, Programming Constructors, Concurrency, Exception handling, Completion.

System Partitioning: Structural versus functional Partitioning. Partitioning issues - Specification Extraction level, Granularity, System Component allocation, Metrics and Estimations, Objective functions and closeness functions, Partitioning Algorithm, Output. Basic Partitioning algorithms - Random mapping, Hierarchical clustering, Multistage Clustering, Group Migration, Radio cut and Simulated Annealing.

Section C

System –Level Design: System design challenges, Abstraction levels, Modeling – Model of computation, system design languages, and system modeling –processor and communication modeling. System models.

Recommended Books:

1. Dainel D.Gajaski., & Abdi, Samer. (2009). *Embedded System Design- Modeling, Synthesis*. New York: Springer Publication.
2. Daniel D. Gajski. (1994). *Specification and Design of Embedded Systems*. New Jersey: PHI Publication.

VLSI 514 High Power Semiconductor Devices

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Get knowledge of power semiconductor devices under extreme operation conditions like high voltage, high current and high temperature which are encountered under typical power electronic environment.
- Understand knowledge developed from this, will help in designing power devices with desired specifications.
- Get knowledge of VMOS, CMOS, DMOS Devices.

Section A

Basic device models: Theory of bipolar and MOS transistors. Small-signal models of bipolar and MOS transistors, Gummel-Poon model. High current effects in diodes: Dependence of lifetime on high-level injection, non-uniform current distribution under high current injection.

Section B

Power biploar transistors: Onset of high-current effects in transistors; Theories of Kirk effect, crowding, pinch-in effects, second breakdown, etc; Emitter geometries for high current and HF operation. SCR: Theories of operation; Relation between shorted emitter and dv/dt ratings; Gate turn-off devices, inverter grade SCRs, special diffusion techniques for SCRs.

Section C

Power VMOS devices, Heat transfer in power devices; Power MOS devices:VMOS&DMOS device structure and models; device packaging.

Recommended Books:

1. Sze, S.M. (1981). *Physics of Semiconductor Devices*. New York: Wiley Publication.

Suggested E-resources:

1. **Basic Device models** by Prof. Roshan Bhosh Department of Electronics and Electrical Communication Engineering Indian Institute of Technology, Kharagpur. https://nptel.ac.in/ courses/117105084/.
2. **Semiconductor Device Modeling** by Prof. Shreepad Karmalkar Department of Electrical Engineering Indian Institute of Technology- Madras, https://nptel.ac.in/courses/117106033/.

VLSI 515 High Speed VLSI Design

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Design Clocked logic styles non clocked logic styles.
- Understand knowledge of circuit designing margining.
- Get knowledge of Clock generation and distribution.

Section A

Clocked Logic Styles, Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic

Non-Clocked Logic Styles, Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families.

Section B

Circuit Design Margining, Design Induced Variations, Process Induced Variations, Application Induced Variations, Noise.

Latching Strategies, Basic Latch Design, and Latching single-ended logic, Latching Differential Logic.

Section C

Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques.

Signalling Standards, Chip-to-Chip Communication Networks, ESD Protection

Clocking Styles, Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

Recommended Books:

1. Bernstein, Kerry. (1999). *High Speed CMOS Design Styles*. New Jersey: Kluwer Academic Publishers.
2. Sutherland, Evan., Stroll,Bob.,& Harris, David.(1999) *Logical Efforts, Designing Fast CMOS Circuits*. Boston, Massachusetts: Kluwer Academic Publishers.
3. Harris, David.(2000*). Skew Tolerant Domino Design*. New Delhi: Elsevier.

Suggested E-resources:

1. **High Speed Devices and Circuits** by Prof. K. N. Bhat Department of Electrical Engineering Indian Institute of Technology, Madras. https://nptel.ac.in/courses/117106089/
2. **CMOS VLSI Circuit** by Prof. A. N. Chandorkar Department of Electrical Engineering Indian Institute of Technology, Bombay. https://nptel.ac.in/courses/117101004/

VLSI 517 Integrated Electronic System Design

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Understanding, gathering and processing of electronics system through basic Motherboard, PCB and IC technologies.
- Design their own circuits based on the knowledge learnt from class.
- Get the opportunity to become proficient in using the 8051 microcontroller for circuit modeling and analysis.

Section A

Electronics Systems; Sensors and Actuators; Microcomputers and Microcontrollers. Packaging of Digital Systems: ICs, PCBs, Chassis and cabinets, Back_ planes and Mother boards, Wires and cables, Connectors.

Section B

Noise in Digital Systems; Clocking and Timing Issues.

Section C

System Design using 8051 Microcontroller (or 68HC12 Microcontroller), Bus based System Design, Real time System Design Issues.

Recommended Books:

1. Burd, S.D. (2001). *System Architectures*. New Delhi: Thomson learning Publication.
2. Cady, F.M. (2009) *Microcontrollers and Microcomputers: Principles of Software and Hardware Engineering*. New York: Oxford University Press.
3. Predko, M. (1998) *Handbook of Microcontrollers*. New York: McGraw-Hill.

Suggested E-resources:

1. **Microprocessors and Microcontrollers** by Prof. Santanu Chattopadhyay Department of E & EC Engineering Indian Institute of Technology, Kharagpur. https://nptel.ac.in/courses/108105102/23
2. **Principles of Communication Systems - Part II** by Prof. Aditya K. Jagannatham Department of Electrical Engineering Indian Institute of Technology, Kanpur. https://nptel.ac.in/courses/108104098/7

VLSI 518 Introduction to MEMS

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Families with the important concepts applicable to MEMS, their fabrication.
- Fluent with the design, analysis and testing of MEMS.
- Describe micro fabrication, micro actuators and surface micromachining and applications.

Section A

Historical Background: Silicon Pressure sensors, Micromachining, MicroElectroMechanical Systems Microfabrication and Micromachining: Integrated Circuit Processes, Bulk Micromachining: Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA)

Section B

Physical Microsensors : Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors Microactuators : Electromagnetic and Thermal microactuation, Mechanical design of microactuators, Microactuator examples, microvalves, micropumps, micromotors-Microactuator systems : Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector

Section C

Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micromachined Systems : Success Stories, Micromotors, Gear trains, Mechanisms Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.

Recommended Books:

1. Senturia, Stephen. D. (2001) *Microsystem Design*. *Norwell, Massachusetts:*Kluwer Academic Publishers.
2. Madou, Marc.(1997). *Fundamentals of Microfabrication*. California: CRC Press.

3. Kovacs, Gregory. (1998) *Micromachined Transducers Sourcebook.* Boston, Massachusetts: WCB McGraw-Hill Publication.
4. Bao, M.-H. (2000). *Micromechanical Transducers: Pressure Sensors, Accelerometers, and Gyroscopes*. New York: Elsevier Publication

Suggested E-resources:

1. **MEMS and Microsystems** Prof. Santiram Kal Department of Electronics and Electrical Communication Engineering Indian Institute of Technology, Kharagpur. https://nptel.ac.in/courses/117105082/4
2. **Microsensors** by Prof. G.K. Ananthasuresh, Department of Mechanical Engineering Indian Institute of Science Bangalore. https://nptel.ac.in/courses/112108092/module1/lec03.pdf

VLSI 519 Low Power VLSI Design

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Learn the design techniques low voltage and low power CMOS circuits for various applications.
- Design and implementation of various design structures of flip flop for low power applications.
- Design the different types of memory circuits and various CMOS static and dynamic logic circuits.
- Understand the mechanisms of power estimation and datapath width adjustment.

Section A

CMOS Device Technology Trends for Power-Constrained Applications, low Power CMOS VLSI Design, Power Estimation - Physics of Power Dissipation in CMOS FET devices, design of low power CMOS Circuits Design and test of low voltage CMOS Circuits.

Section B

Flip-Flop and clock Networks Design Methods forlow power, Introduction to low Power Memory Design, Low Power Static ram architectures, low - power Memory design SRAM/DRAM Design

Section C

Power estimation, synthesis for low power, power optimization by Data Path Width adjustment.

Recommended Books:

1. Roy, Kaushik. & Prasad, Sharat. C. (2009). *Low Power CMOS VLSI Circuit Design*. Dublin: Willey Publications.
2. Pal, Ajit. (2015). *Low Power VLSI Circuits and Systems*. New Delhi: Springer Publications.
3. Pedramand, M.,& Rabaey, J.M.(2002) *Power Aware Design Methodologies*. Boston, Massachusetts: Kluwer Academic Publishers.
4. Kang, Sung – Mo., & Leblebici, Yusuf. (2002). *CMOS Digital Integrated circuits- Analysis and Design*. New Delhi: TMH Publications.

Suggested E-Resources:

1. **Low Power VLSI Circuits and Systems** by Prof. Ajit Pal, Department of Computer Science and Engineering, IIT Kharagpur. https://nptel.ac.in/syllabus/106105034/

VLSI 520 Nanoelectronics

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Get knowledge in electronics has been driven by miniaturization.
- Understand CMOS and MOSFET scaling.
- Understand the electronic properties of molecules, carbon nanotubes and crystals.

Section A

Shrink-down approaches: Introduction, CMOS Scaling, The nanoscale MOSFET, Finfets, Vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.),

Section B

Resonant Tunneling Transistors, Single electron ,transistors, new storage, optoelectronic, and spintronics devices.

Atoms-up approaches: Molecular electronics involving single molecules as electronic devices, transport in molecular structures, molecular systems as alternatives to conventional electronics.

Section C

Molecular interconnects; Carbon, nanotube electronics, bandstructure& transport, devices, applications.

Recommended Books:

1. Poole , C.P., & Owens, F.J. (2003). *Introduction to Nanotechnology*. New York: Wiley Publications.
2. Waser, R. (Ed.). (2012). *Nanoelectronics and information technology.* John Wiley & Sons.
3. Drexler, K.E. (1992). *Nanosystems*. New York: Wiley Publications.
4. Davies, John. H. (1998). *The Physics of Low-Dimensional Semiconductors*. New York: Cambridge University Press.

Suggested E-resources:

1. **Nanostructures and Nanomaterials: Characterization and Properties** by Prof. Anandh Subramaniam and Prof. Kantesh Balani Department of Materials Science & Engineering Indian Institute of Technology, Kanpur. https://nptel.ac.in/courses/ 118104008/
2. **Nanoelectronics: Devices and Materials** by Prof. Navakanta Bhat Centre for Nano Science and Engineering Indian Institute of Science, Bangalore. http://textofvideo.nptel.ac.in/117108047/ lec1.pdf

VLSI 537 Photonics Integrated Circuits

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Describe the optical waveguides and optical couplers with the help of coupled mode theory.

- Explain the basic operating mechanisms of optical switches and modulators.
- Identify the performance limiting factors and applications of integrated optics.

Section A

Optical Waveguide Modes, Planar Waveguides, Symmetric and Asymmetric, Slab and channel waveguides, Optical Couplers: Prism Couplers, Gräting Couplers, Tapered Couplers, Fiber to Waveguide Couplers, Multilayer Planar Waveguide Couplers, Dual-Channel Directional Couplers, Coupled-Mode Theory.

Section B

Electro-Optic Modulators: Basic Operating Characteristics of Switches and Modulators, the Electro-Optic Effect, Single-Waveguide Electro-Optic Modulators, Dual-Channel Waveguide Electro-Optic Modulators. Acousto-Optic Modulators: Acousto-Optic Effect, Raman-Nath-and Bragg Type Modulators, Acousto-Optic Frequency Shifters.

Section C

Distributed-Feedback Lasers: Theoretical Considerations and performance characteristics, Integrated Optical Detectors: Depletion Layer Photodiodes, Specialized Photodiode Structures, Techniques for Modifying Spectral Response, performance limiting factors. Applications of Integrated Optics and Current Trends: Opto-Electronic Integrated Circuits and future projections.

Recommended Books:

1. Hunsperger, Robert. G. (1995). *Integrated Optics Theory and Technology*. Berlin, New York: Springer.
2. Nishihara, Hiroshi. Haruna, Masamitsu.,& Suhara, Toshiaki. (1989). *Optical integrated circuits*. New York: McGraw-Hill Publication.
3. Reed, Graham. T., & Knights, Andrew. P. (2004). *Silicon photonics: An Introduction*. New York: John Wiley & Sons.
4. Tamir,T.(1990). *Guided wave Opto-electronics*. Berlin, Heidelberg: Springer.

Suggested E- resource:

1. **Photonic Integrated Circuits** by Dr. Srinivas Talabatulla, Department of Electronics & Communication Engineering, IISc, Bangalore. https://nptel.ac.in/courses/117108142/

VLSI 523 Representation and Analysis of Random Signals

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Understand the theory and application of probability, random variables and random processes
- Understand to study and analyze analytical expression

Section A

Random variable, distribution functions and probability densities-Expected value and moments of random variables-coefficient of variation, skewness and kurtosis-of random variables conditional mean and variance-moment generating function. Discrete random variables and their distribution - Binomial, Negative Binomial, Hyper geometric and multinational distributions-Poisson distribution Relationship between distributions of various discrete type random variables.

Section B

Continuous random variable and their distribution- Normal, Lognormal , multivariate normal distribution , _gamma, exponential, Chi-square, Weibull , Rayleigh distribution Relationship between distribution of various continuous type random variables. Stochastic processes-classification Stationary processes-Independent increment processes- Markov processes - counting processes- Narrow -band process- Stochastic processes for analysis of physical phenomena- Normal (Gaussian), Weiner- Levy , Poisson Bernoulli and shot noise processes -Auto correlation function.

Section C

Transformation of single random variable- Transformation of several random variable function of random variables- Sum, Difference, product and ratio of random variable- Transformation through characteristic function.

Recommended Books:

1. Ochi, Michel .K. (1990) *Applied Probability and Stochastic Processes in Engineering and Physical Sciences*. New York: Wiley Publications.
2. Papoulis, A. (2002). Probability, Random Variables and Stochastic Processes. New York: TMH Publications.
3. Trivedi ,K.S. (2001). *Probability and Statistics with Reliability, Queuing and Computer Science Application*. New York: Wiley Publications.

VLSI 526 Speech Signal Processing

Max. Marks : 100	**L**	**T**	**P**	**C**
(CA: 40+ ESA: 60)	**4**	**0**	**0**	**4**

Learning Outcomes: After successful completion of this course, students will be able to:

- Describe the fundamentals of digital speech processing and digital model for speech signal process.
- Illustrate and analyze the time domain model and Fourier representation for speech processing.
- Explain basic principles of LPC equations and solutions.

Section A

Introduction to digital speech processing, digital transmission and storage of speech, speech synthesis system, speaker verification and identification, speech recognition system.Digital models for speech signal process of speeds production, Acoustic theory of speech production, Digital models for speech signals.

Section B

Time domain models for speech processing, Digital representation of speech waveform. Short-time Fourier analysis, Homo-morphic speech processing.

Section C

Linear predictive coding ,basic principles of linear predictive analysis, computation for gain, solution of LPC equations, comparison between methods of solution of the LPC analysis equation ,Prediction error signals, Frequency domain linear predictive analysis ,speech parameters and their relationships, Application LPC parameters.

Recommended Books:

1. Rabiner, L.R., & Schafer, R.W. (1978). *Digital Processing of Speech Signals*. New Delhi: PHI Publications.
2. Plett, C.,Rogers, J.W.M., &Copeland, M.A. (2003). *Radio Frequency Integrated Circuit.* New Jersey: Design Artech House Publishers.
3. Best, R.E. (2003). *Phase-Locked Loops: Design, Simulation and Application*. New York: TMH Publication.

4. Deller, J.R., HansenJ.H.L ., & Proakis, J.G. (1999). *Discrete-time processing of Speech Signals*. New York: Wiley-IEEE Press.
5. Quatieri, T.F. (2001). *Discrete-Time Speech Processing: Principles and Practices*. Massachusetts: PHI Publications.

Suggested E-resource:

1. **Digital Speech Processing** by Prof. S. K. Das Mandal Centre for Educational Technology Indian Institute of Technology, Kharagpur .https://nptel.ac.in/courses/117105145/19

Reading Electives

VLSI 605R Advanced Electronic Packaging

Max. Marks : 100	**L**	**T**	**P**	**C**
(ESA: 100)	**0**	**0**	**4**	**2**

This course is designed to equip students with the required knowledge and concepts in mechanical, thermal, and reliability concern of modern electronic packaging. Emphasis is on IC packaging performance and its achievement through the proper material selection. The course will explore the multichip module, electrical autonomy IC assembly, challenges in the electronic packaging, and can recognize the various methods available and selection of appropriate packaging solution for particular applications.

Suggested e-resource:

1. **An Introduction to Electronics Systems Packaging** by IISC Bangalore. https://nptel.ac.in/courses/108108031/

VLSI 606R Compound Semiconductor Technology

Max. Marks : 100	**L**	**T**	**P**	**C**
(ESA: 100)	**0**	**0**	**4**	**2**

This course provides students with the basic understanding of Non-Silicon MOSFET technology. The students should be able to use properties and trade-offs of compound semiconductors (GaAs, InAs, InP and InSb) for design of high performance MOSFETs. The students will be able to explain the challenges and power performance of strained III-V MOSFETs, the high k dielectric based MOSFETs. Students should also be able to discuss the Future Scaled CMOS and hybrid CMOS technology.

Suggested e-resources:

1. **Nanoelectronics: Devicesand Materials** by Prof. K. N. Bhat Centre for Nano Science and Engineering. https://nptel.ac.in/ courses/117108047/28.
2. **Compound Semiconductor Devices** by Prof. C. G. Fonstad, MIT, USA. https://ocw.mit.edu/courses/electrical-engineering-and-computer-science/6-772-compound-semiconductor-devices-spring-2003/lecture-notes/.

VLSI 601R High Level Synthesis

Max. Marks : 100	**L**	**T**	**P**	**C**
(ESA: 100)	**0**	**0**	**4**	**2**

This course expose students to the advanced HDL design techniques, methodology and industrial standard EDA tools in electronic design. This course also discusses the new ideas and techniques in high level synthesis, essential issues in synthesis, architectural model, and guidelines for HDL design. Students will be expected to explore design methodology for high level synthesis, chip synthesis and physical design methodology.

Suggested e-resource:

1. **High level Synthesis** by IIT Guwahati. https://nptel.ac.in/courses/ 117103125/4.
2. **Synthesis of Digital Systems** by Dr. Preethi Ranjan Panda, Department of Computer Science & Engineering, Indian Institute of Technology, Delhi. https://nptel.ac.in/courses/106102181/7

VLSI 604R VLSI Testing and Design for Testability

Max. Marks : 100	**L**	**T**	**P**	**C**
(ESA: 100)	**0**	**0**	**4**	**2**

The course attempts to expose the students to the most recent, yet fundamental, VLSI test principles in an effort to help them design better quality products that can be reliably manufactured in large quantity. The course explores the issue related to the physical defects, test generation technique for combinational and sequential circuits, controllability and observability and redundancy.

Suggested e-resources:

1. **Digital VLSI Testing** by Prof. Santanu Chattopadhyay Department of Electronics and Electrical Communication Engineering, IIT Kharagpur. https://onlinecourses.nptel.ac.in/noc17_ec02/preview.
2. **Testing and Verification of VLSI Circuits** by Prof. Virendra Singh IIT Mumbai. https://www.ee.iitb.ac.in/~viren/Courses/2012/EE709.htm

Online Reading Electives

Digital Image Processing

This course provides an introduction to basic concepts, methodologies and algorithms of digital image processing focusing on image analysis and image enhancement and restoration for easier interpretation of images. The course provides overview of digital image processing including visual perception, Image Digitization, Basic Transformations, Interpolation and Resampling, Image Interpolation, Image Transformation, Image Enhancement, Image Segmentation, Morphology, Object Representation and Description, object Recognition etc. The course focuses on to create an ability in students to analyze a problem in this domain and identify the computing requirements appropriate for its solution; an ability to design, implement and evaluate a computer-based system, process, component or program to meet desired needs.

Suggested e-resource:

1. **Digital Image Processing** by Prof. P. K. Biswas, IIT Kharagpur. https://nptel.ac.in/courses/117105079/

Organic Electronic Devices

Organic electronic devices are quickly making their way into the commercial world, with innovative thin mobile devices, high-resolution displays, and photovoltaic cells. Purpose of the course is to learn about this highly promising technology, which is based on small molecules and polymers, and to discuss how these materials can be implemented successfully in established organic electronic modules. In this course students will gain the ability to tie molecular transport phenomena with macroscopic device response such that you will be well-prepared to analyse troubleshoot, and design the next generation of organic electronic materials and devices.

Suggested e-resources:

1. **Organic Electronic Devices** by Dr. Bryan W. Boudouris, Purdue University. https://www.edx.org/course/organic-electronic-devices-purduex-nano515x

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